
Intel
Developer
Forum
designing
platform
solutions
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Intel Developer Forum

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Intel Corporation

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Agenda

- New Technologies
- Compelling Products for Every Segment
- Summary

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Agenda

- New Technologies
  - Silicon Technology
  - Validation Technology
  - Katmai New Instructions
- Compelling Products for Every Segment
- Summary

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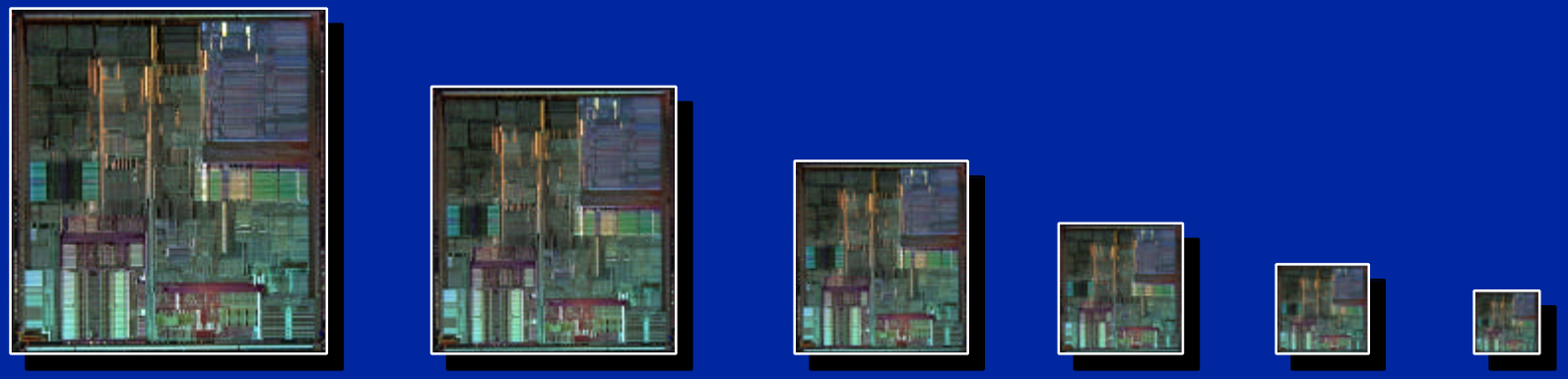
Technology Trends



Line Width Shrinks

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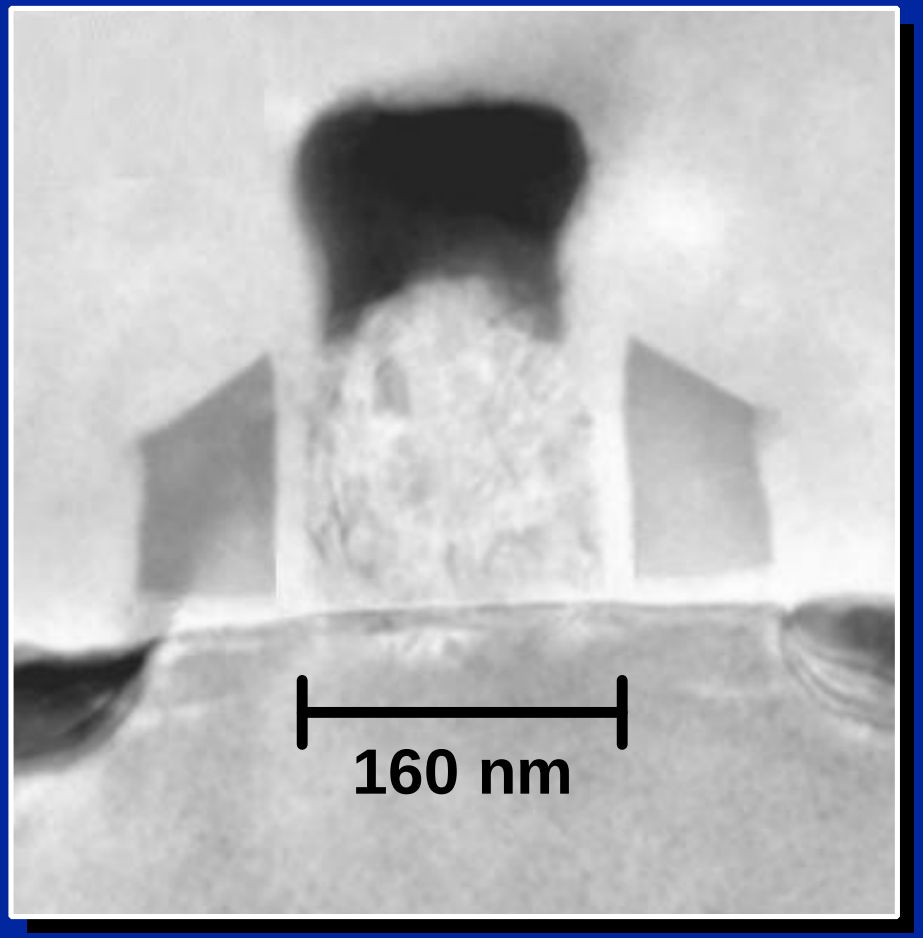
0.18 µm Logic Technology



Transistor

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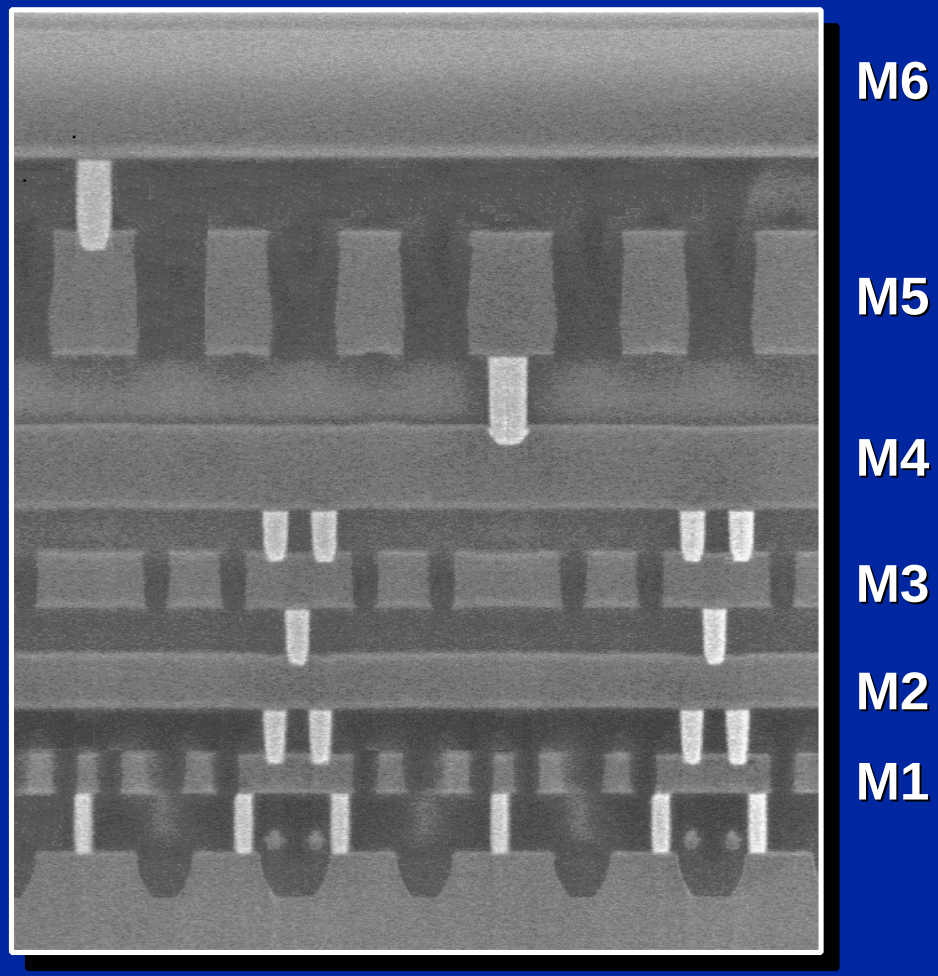
0.18 µm Logic Technology



Interconnects

Agenda

- New Technologies
  - Silicon Technology
  - Validation Technology
  - Katmai New Instructions
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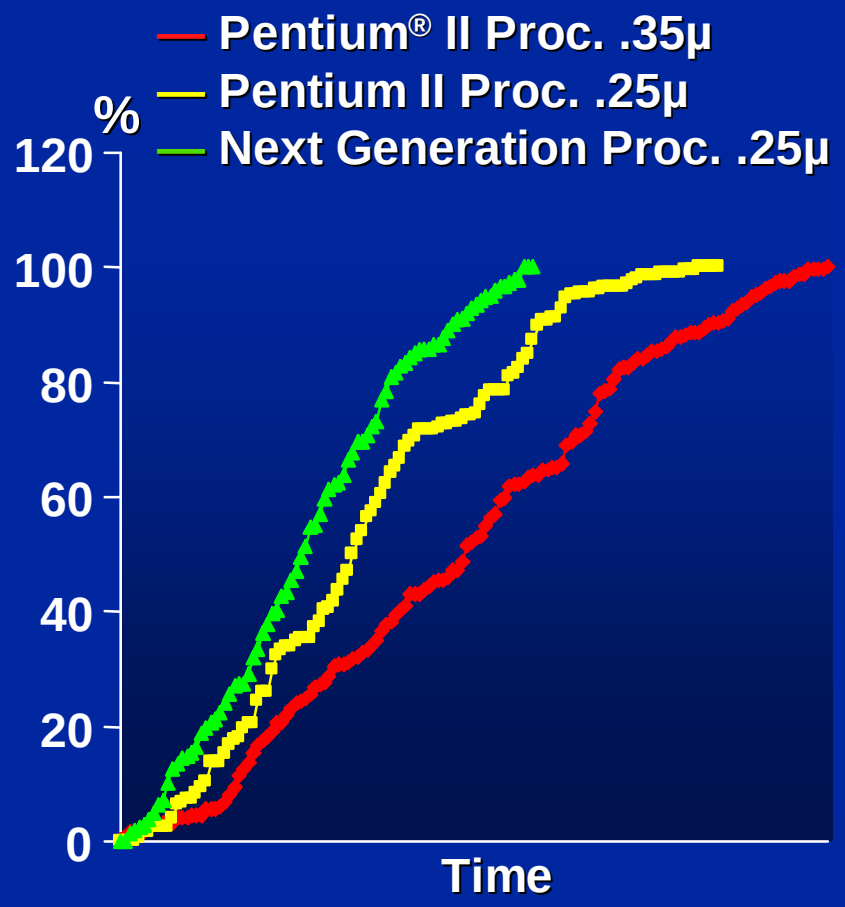
Validation Technology

- Design for correctness
  - Formal verification
  - Cluster level validation
  - System level co-simulation
- The big test
  - Thorough 24X7 testing
  - Coverage based testing
  - Segment specific stresses (servers, desktop, mobile…)



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Validation Technology

- **Stress testing:**
  - **124 Intel servers & 1072 clients**
  - **>50K stress hours**
  - **>30 Miles of Cat5 Network, multiple protocols**
  - **>30 stress workloads, >30 system configurations**
  - **Win NT*, Win '9X*, Win 3.x, OS/2*, SCO*, Unix*, Netware*, Unixware***
  - **75 x 10^{18} cycles**

Agenda

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Katmai New Instructions

- New architecture enhancements
  - Increase performance
  - Reduce system bottlenecks
- Improved handling of rich data types
  - Real-time MPEG2 encode/decode
  - Faster, richer 3D graphics
  - AC3 audio
  - Continuous, accurate speech recognition
  - Complex imaging effects
  - Realistic movement physics

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Katmai New Instructions

Dynamic Execution

Multi-Transaction P6 Bus

MMX™ Technology

Current P6 Microarchitecture

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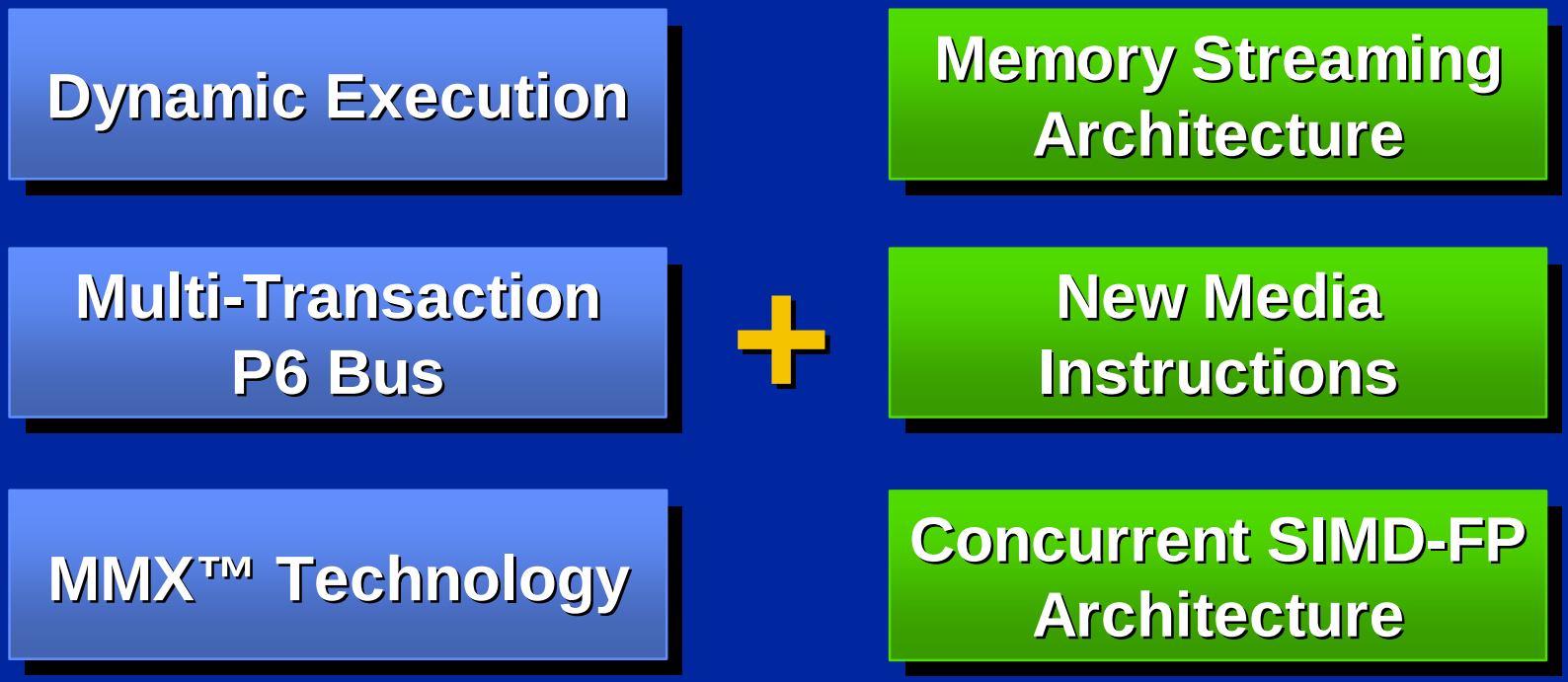
Katmai New Instructions



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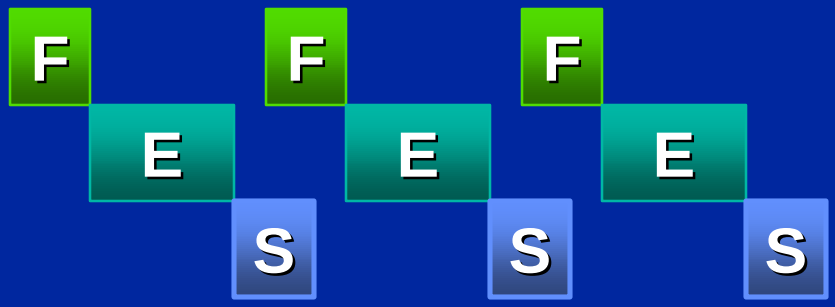
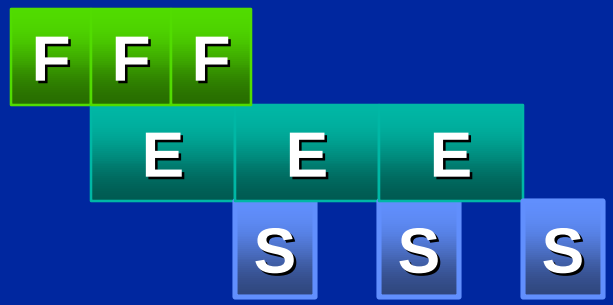
Memory Streaming Benefits

Without Memory Streaming



With Memory Streaming



Time

Streaming Hides Memory Latency Under Software Control

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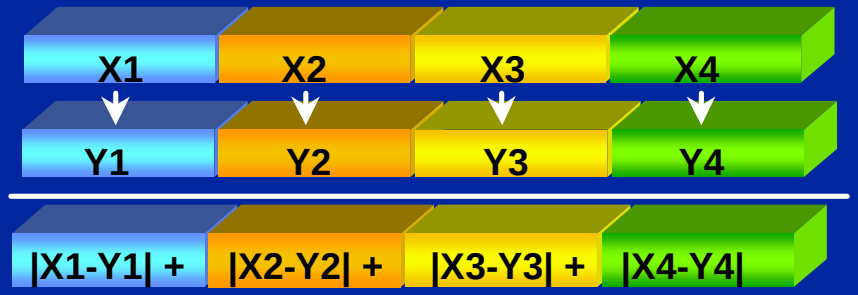
New Media Instructions

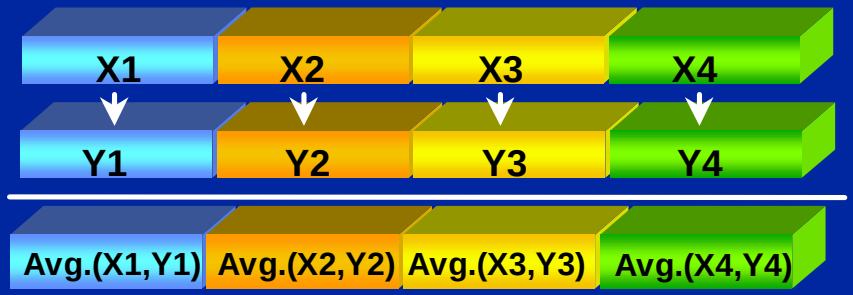
Sum of Absolute Differences

Video encode: motion estimation



Average w/Rounding down

Video decode: motion compensation



Additional New Media Instructions

- Packed Maximum
- Packed Minimum

  Speech Recognition

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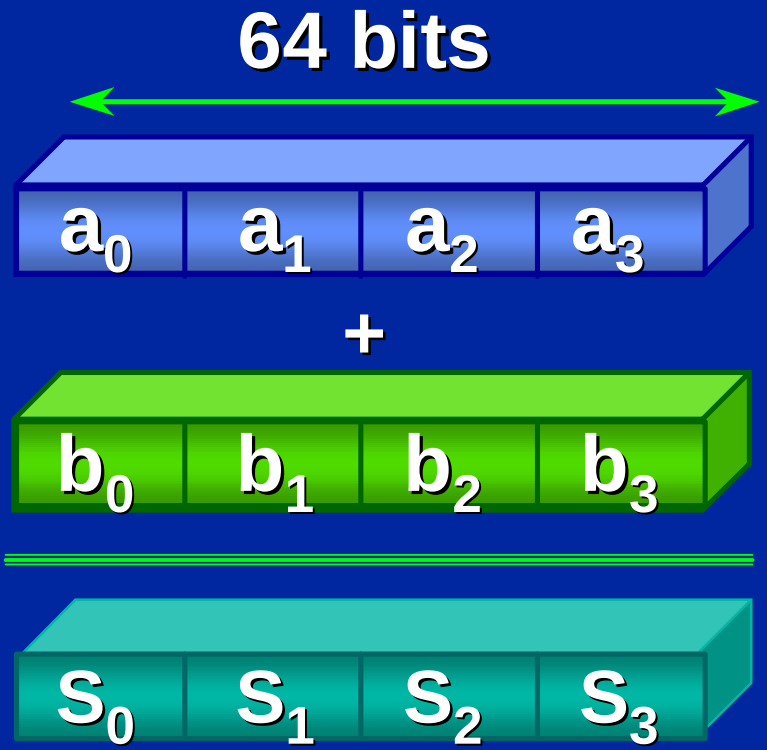
MMX™ Technology



where:
$s_n = a_n + b_n$

Packed Integer Op./Instruction

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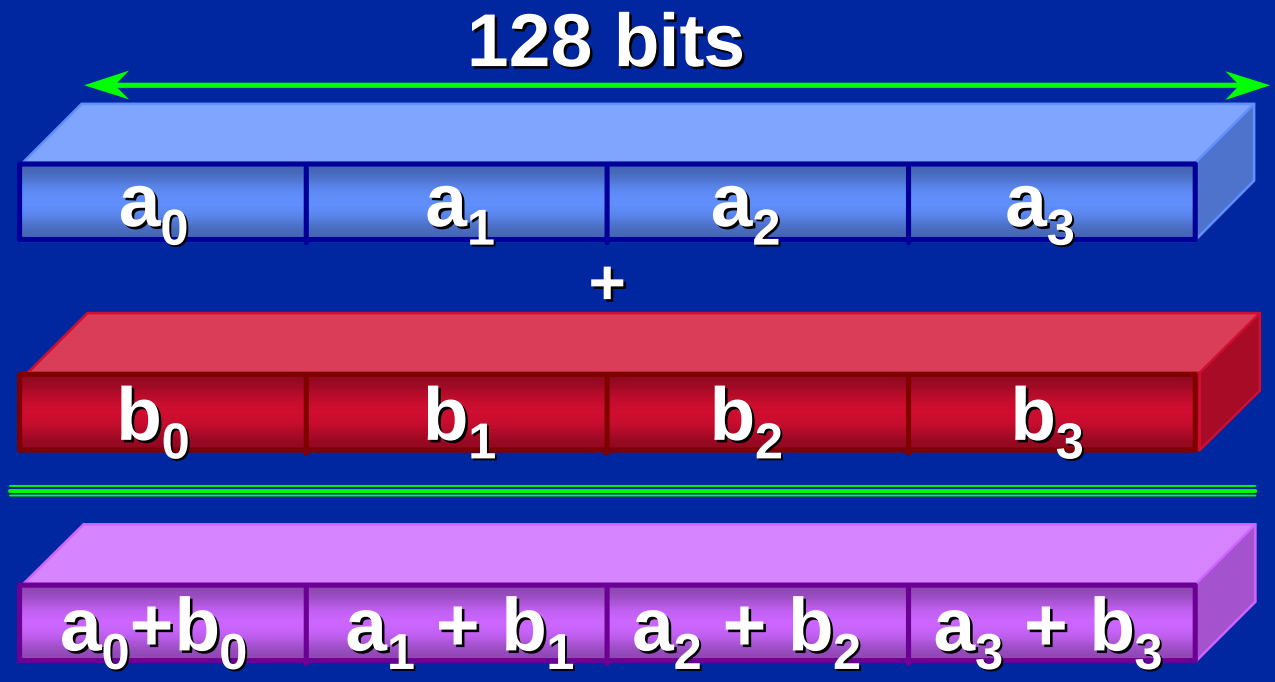
DEMO

Katmai New Instructions
SIMD Architecture for FP Data



4-wide Single Precision Packed
Single Op./Instruction

intel® ***500MHz Katmai/Tanner = 2 GFlops/sec Peak***

Agenda

- New Technologies
- **Compelling Products for Every Segment**
- Summary

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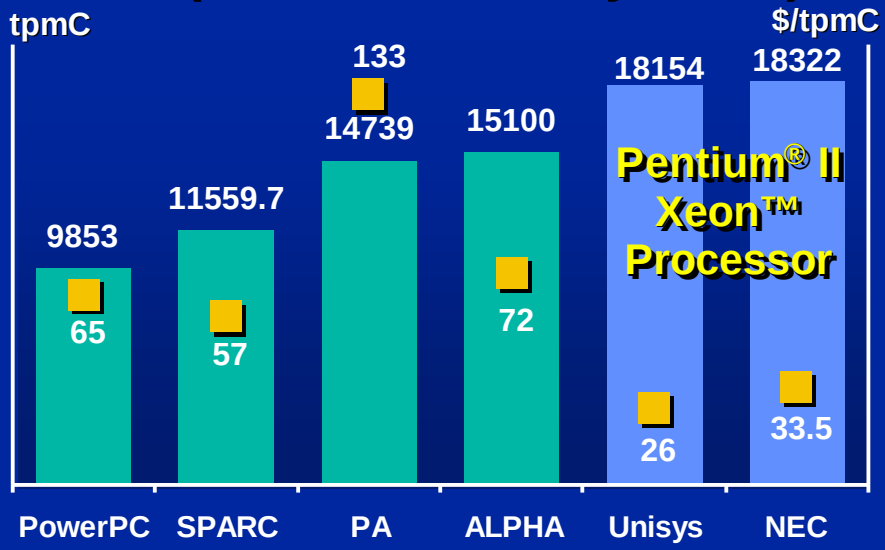
Server/Workstation

	Pentium® II Xeon™ Processors
Launch	1998
Processor	Pentium II Xeon
L2 Cache	512K,1M, (2M)
Frequency	400/450 MHz
Package	S.E.C.C.
Chipset/Bus	450NX/100 440GX/100

Performance and Value: OLTP (TPC-C, 4 CPU Systems)



Source for Sun, HP, IBM and Compaq results: TPC Website (www.tpc.org). Pentium II Xeon processor performance measurements audited and submitted by Unisys and Compaq to TPC 6/29/98. TPC-C is a benchmark from the Transaction Processing Council (TPC Benchmark™ C).

Server/Workstation

	Pentium® II Xeon™ Processors	Tanner Processors
Launch	1998	1H'99
Processor	Pentium II Xeon	Tanner (0.25µ)
L2 Cache	512K,1M, (2M)	512K, 1M, 2M
Frequency	400/450 MHz	500 MHz
Package	S.E.C.C.	S.E.C.C.
Chipset/Bus	450NX/100 440GX/100	450NX/100 440GX/100

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Server/Workstation

	Pentium® II Xeon™ Processors	Cascades Processors
Launch	1998	2H'99
Processor	Pentium II Xeon	Cascades (0.18µ)
L2 Cache	512K,1M, (2M)	TBD
Frequency	400/450 MHz	>500 MHz
Package	S.E.C.C.	S.E.C.C.
Chipset/Bus	450NX/100 440GX/100	TBD

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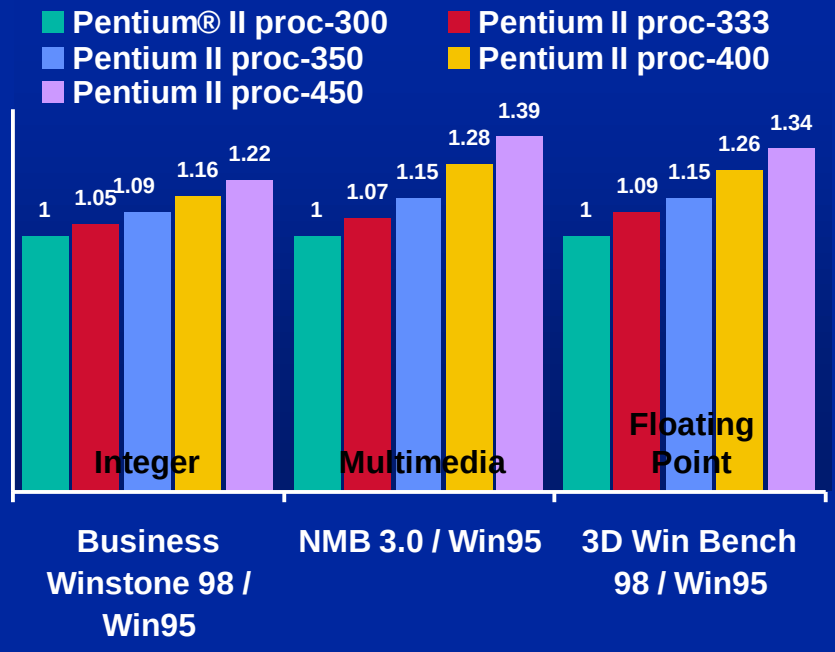
Performance PC

	Pentium® II Processors
Launch	1998
Processor	Pentium II
L2 Cache	512K BSRAM
Frequency	350,400,450 MHz
Package	S.E.C.C.
Chipset/Bus	440BX/100



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Source: Intel MAP. Performance PC Configuration: Intel SE440BX Motherboard; 32MB SDRAM, Seagate SCSI disk, Matrox Millennium II/AGP, 3D Win Bench measured on STB Velocity 128/AGP; Microsoft DirectX 5; L2 ECC Disabled.

Performance PC

	Pentium® II Processors	Katmai Processors
Launch	1998	1H'99
Processor	Pentium II	Katmai (0.25µ)
L2 Cache	512K BSRAM	512K BSRAM
Frequency	350,400,450 MHz	450 & 500 MHz
Package	S.E.C.C.	S.E.C.C. & S.E.C.C.2
Chipset/Bus	440BX/100	440BX/100

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Performance PC

	Pentium® II Processors	Coppermine Processors
Launch	1998	2H'99
Processor	Pentium II	Coppermine (0.18µ)
L2 Cache	512K BSRAM	TBD
Frequency	350,400,450 MHz	>500 MHz
Package	S.E.C.C.	S.E.C.C.2
Chipset/Bus	440BX/100	TBD

DEMO

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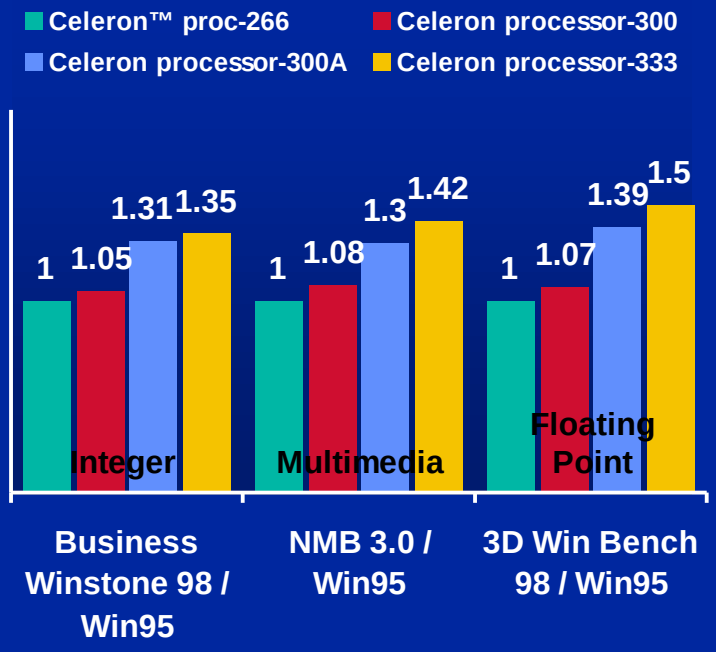
Basic PC

	Celeron™ Processors
Launch	1998
Processor	Celeron ™
L2 Cache	128K Integrated
Frequency	300A,333 MHz
Package	SEPP
Chipset/Bus	440LX/EX



Source: Intel MAP. Basic PC Configuration: Celeron on 440EX, PP/MT on 430TX; 32MB SDRAM, Seagate EIDE disk, ATI 3D Rage Pro; 3D Winbench measured on STB Velocity 128; Microsoft DirectX 5.

Basic PC

	Celeron™ Processors	Celeron™ Processors
Launch	1998	1H'99
Processor	Celeron ™	Celeron ™
L2 Cache	128K Integrated	128K Integrated
Frequency	300A,333 MHz	366 MHz
Package	SEPP	SEPP/PPGA
Chipset/Bus	440LX/EX	440LX/EX

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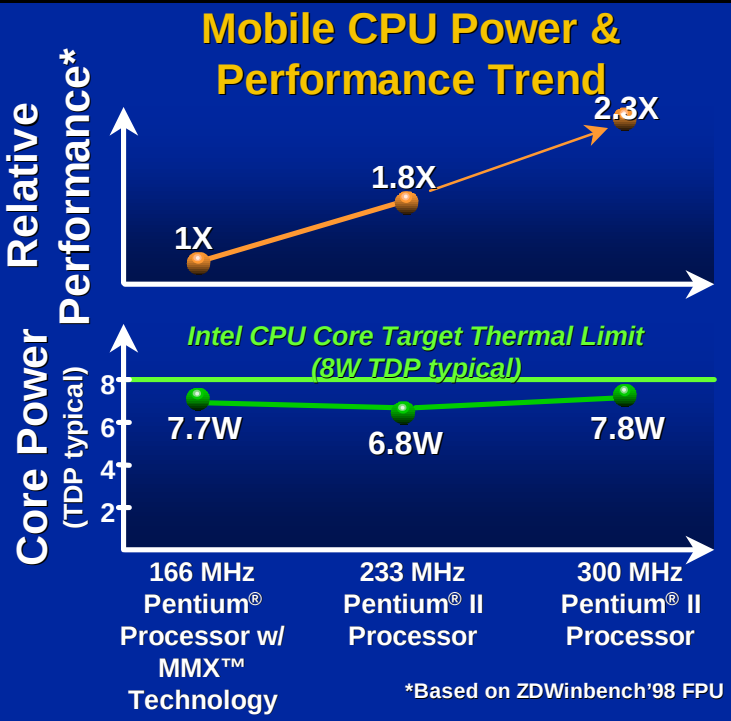
Mobile PC

	Mobile Pentium® II Processors
Launch	1998
Processor	Mobile Pentium II
L2 Cache	512K PBSRAM
Frequency	233,266,300 MHz
Package	Mini-Cartridge Module
Chipset/Bus	440BX/66



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*Mobile Pentium® processor with MMX™ technology at 166/200/233/266 MHz ran on Gateway*Solo9100* system with Intel 430TX/PCIset-based mobile module, 512K L2 cache, 32MB SDRAM, 2.1GB HDD, 8X-20Xmax CD-ROM, C&T 65554 graphics controller; Mobile Pentium® II processor 300/266/233 MHz ran on Gateway* Solo 2500 w/ Intel 440BX mobile module, 512K L2 cache, 32MB SDRAM, 2.1GB HDD, 8X-20Xmax CD-ROM, MagicGraph*128XD graphics controller.

Mobile PC

	Mobile Pentium® II Processors	Mobile Pentium® II Processors
Launch	1998	1H'99
Processor	Mobile Pentium II	Mobile Pentium II
L2 Cache	512K PBSRAM	TBD
Frequency	233,266,300 MHz	>333 MHz
Package	Mini-Cartridge Module	Mini-Cartridge Module
Chipset/Bus	440BX/66	440BX/66

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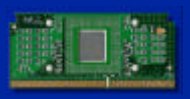
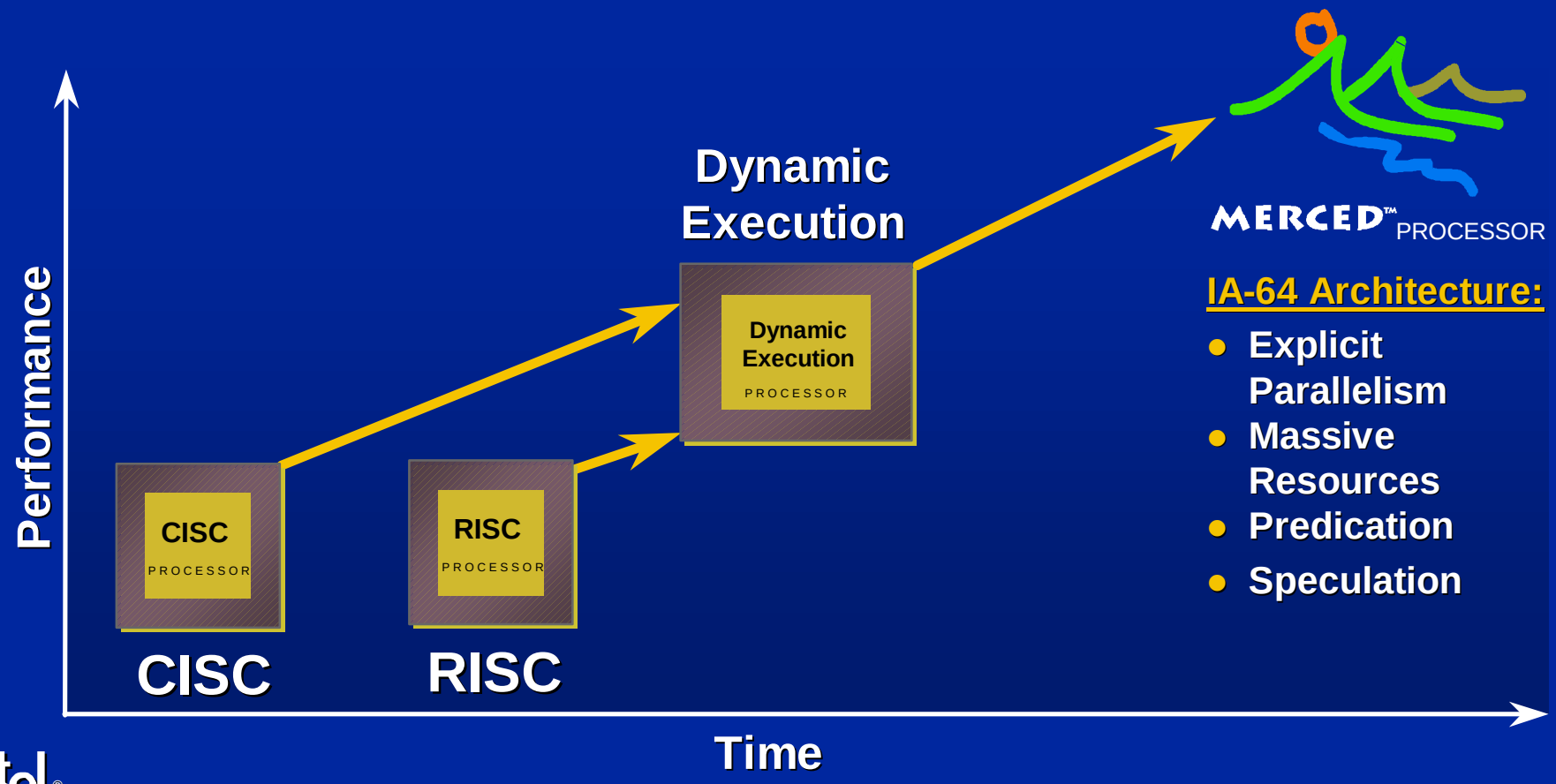
Segmented Product Roadmap

	'98	'99
 Server/ Workstation	Pentium® II Xeon Processors	Tanner and Cascades Processors
 Performance PC	Pentium® II Processors	Katmai and Coppermine Processors
 Basic PC	Celeron™ Processors	Celeron™ Processors
 Mobile PC	Mobile Pentium® II Processors	Mobile Pentium® II Processors
 Set Top Box Handheld	StrongARM* Processors	StrongARM* Processors

IA-64 Architecture: EPIC Technology

Explicitly Parallel Instruction Computing



IA-64 Architecture:

- Explicit Parallelism
- Massive Resources
- Predication
- Speculation

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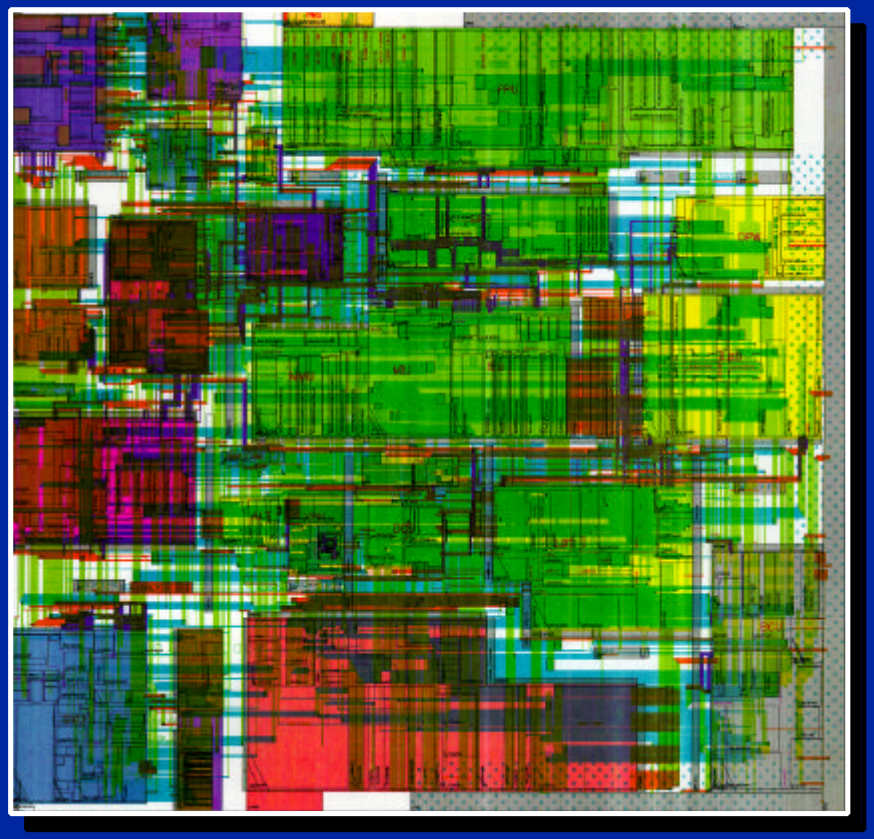
Merced™ Processor: The Entry Product for IA-64

- **Program Status:**
  - Logic design complete
  - Circuit design and layout meeting tapeout milestones
  - OEM platform designs on track for first samples
  - Compiler maturity progressing
  - Software development kits shipping



Merced Processor Floorplan

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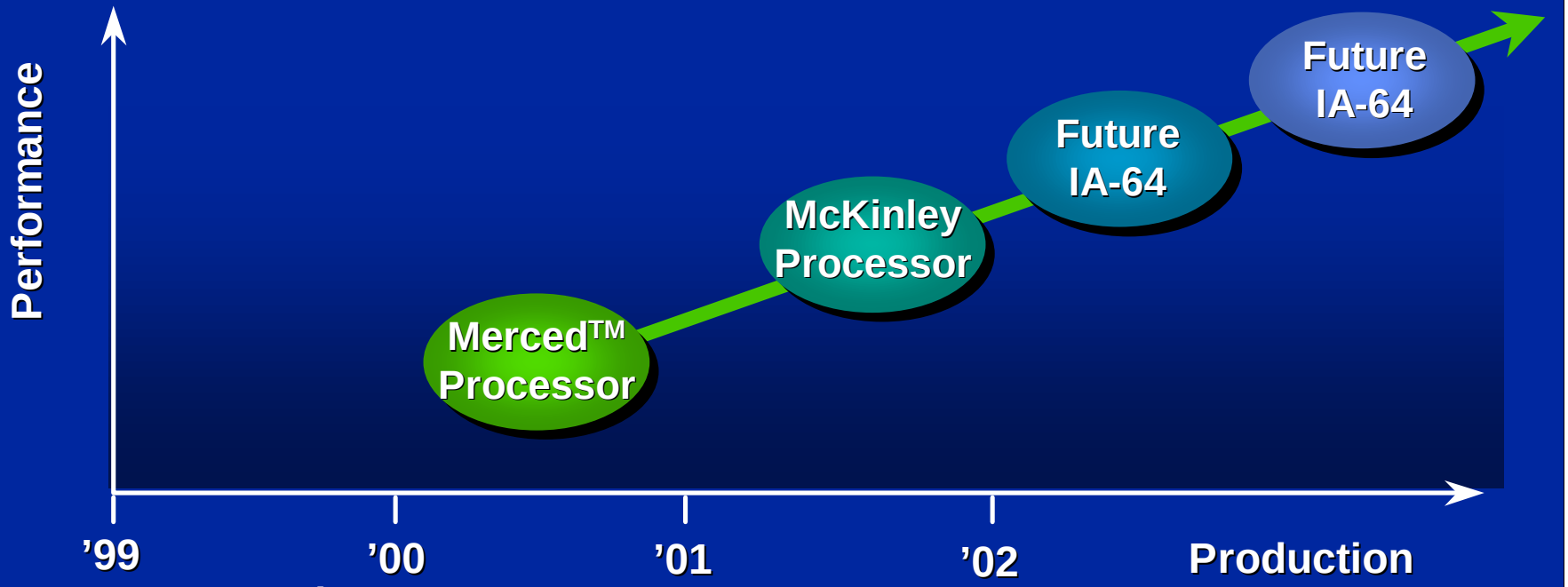
On Track for Production in Mid-2000

IA-64 Processor Roadmap



- Merced Processor:
  - Entry product for the IA-64 product family
  - Full IA32 Software Compatibility
  - Compelling Features, Scalability, RASUM and Performance
  - On track for mid-2000 production
- McKinley Processor:
  - Performance ~2x Merced processor
  - Production targeted for 2H'01

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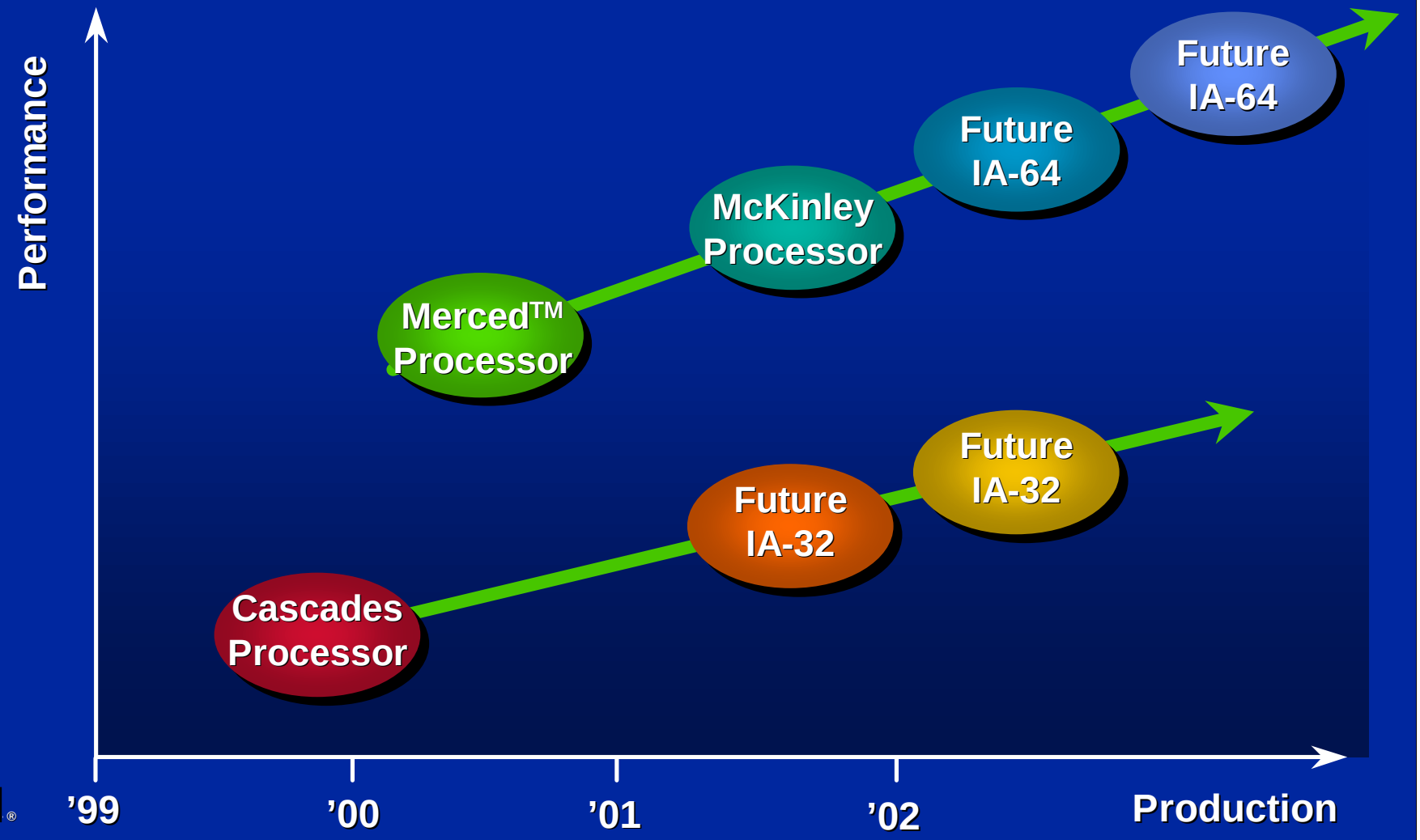
Server/Workstation Processor Roadmap



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Summary

- Intel provides leading edge Technologies
  - Silicon Technology
  - Validation Technology
  - Katmai New Instructions
- Intel's roadmap has never looked stronger
- Build your successful business with our compelling products

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Intel
Developer
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